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09/729,010	12/04/2000	Michael Ficco	PD-200235	6750

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EXAMINER	
HOFFMAN, BRANDON S	

ART UNIT	PAPER NUMBER
2136	

DATE MAILED: 09/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/729,010	FICCO, MICHAEL	
	Examiner	Art Unit	
	Brandon S. Hoffman	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *70-91* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *70-91* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 70-91 are pending in this office action.

Rejections

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 70-74 and 82-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boutaud et al. (U.S. Patent No. 5,734,927) in view of Tsukamoto et al. (U.S. Patent No. 5,796,828).

Regarding claim 70, Boutaud et al. teaches an apparatus for storing and retrieving digital video data, comprising:

- A plurality of multiplexers, each configured to receive an associated one of the plurality of data bits in the data bit pattern and its inverse (fig. 10D, ref. num 4380 and 4390), and configured to output one of the associated one of the plurality data bits or its inverse according to a preprogrammed bit altering scheme (fig. 10D, ref. num 4378), the output of each of the plurality of multiplexers being combined to form an altered data bit pattern.

Boutaud et al. does not teach an interface couple to a system bus and configured to receive from the system bus a plurality of data bits arranged in a data bit pattern; and a storage device coupled to the interface and configured to store the altered data bit pattern.

Tsukamoto et al. teaches an interface couple to a system bus and configured to receive from the system bus a plurality of data bits arranged in a data bit pattern (fig. 2, ref. num 103 and 20); and a storage device coupled to the interface and configured to store the altered data bit pattern (fig. 2, ref. num 23A, 24, and 40).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine receiving data bits and storing the altered data bits, as taught by Tsukamoto et al., with the apparatus of Boutaud et al. It would have been obvious for such modifications because in a DVR application, data bits are required to be stored for later retrieval and viewing. Storing the bits in a scrambled form prevents anyone from illegally viewing the program.

Regarding claims 71 and 72, Boutaud et al. as modified by Tsukamoto et al. teaches wherein the plurality of multiplexers are implemented in at least one of a hardware device, discrete logic device, or a software device (see fig. 10D, ref. num 4380 and 4390, the muxes are hardware based), wherein the hardware device is at least one of a field-programmable gate array, or an ASIC (the examiner takes official

notice that the hardware device is a FPGA or an ASIC because the hardware device could be swapped for another FPGA or ASIC if security were to be compromised.).

Regarding claim 73, Boutaud et al. as modified by Tsukamoto et al. teaches wherein the preprogrammed bit altering scheme is based upon at least one of a serial number or a random number (see fig. 2, ref. num 27 of Tsukamoto et al., the clock is random).

Regarding claim 74, Boutaud et al. as modified by Tsukamoto et al. teaches wherein the plurality of multiplexers are each further configured to receive, from the storage device, an associated one of the plurality of data bits in the altered data bit pattern and its inverse, and configured to select one of the data bits in the altered data bit pattern or its inverse according to the preprogrammed bit altering scheme, the output of each of the plurality of multiplexers being combined to restore the data bit pattern (see fig. 10D, ref. num 4380 and 4390 of Boutaud et al. and fig. 2, ref. num 25 of Tsukamoto et al.).

Regarding claim 82, Boutaud et al. teaches a method for storing and retrieving digital video data within a storage device, comprising:

- Inputting into at least one multiplexer, an associated one of the data bits and its inverse for each of the data bits forming the bit pattern (fig. 10D, ref. num 4380);

- Altering the bit pattern of the data bits to form an altered bit pattern by selecting one of the associated one of the data bits or its inverse for each of the data bits forming the bit pattern based upon a preprogrammed data altering scheme to form the altered bit pattern (fig. 10D, ref. num 4378); and
- Restoring the altered bit pattern to the bit pattern by inputting into the multiplexer, an associated one of the altered data bits and its inverse for each of the data bits in the altered bit pattern, and selecting one of the associated one of the altered data bits or its inverse based upon the preprogrammed data altering scheme (the reverse process would hold true to restore the data).

Boutaud et al. does not teach receiving data bits across a bus, the data bits forming a bit pattern, storing the altered bit pattern and outputting the restored data bits.

Tsukamoto et al. teaches receiving data bits across a bus, the data bits forming a bit pattern (fig. 2, ref. num 103 and 20); storing the altered bit pattern (fig. 2, ref. num 23A, 24, and 40); and outputting the restored data bits (fig. 2, ref. num 26 and 105).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine receiving data bits, storing the altered data bits, and outputting the bits, as taught by Tsukamoto et al., with the apparatus of Boutaud et al. It would have been obvious for such modifications because in a DVR application, data bits

are required to be stored for later retrieval and viewing. Storing the bits in a scrambled form prevents anyone from illegally viewing the program.

Regarding claims 83 and 84, Boutaud et al. as modified by Tsukamoto et al. teaches wherein the plurality of multiplexers are implemented in at least one of a hardware device, discrete logic device, a software device, a field-programmable gate array, or an ASIC (see fig. 10D, ref. num 4380 of Boutaud et al.), and the altering and restoring are unique to the storage device (see fig. 2, ref. num 27 of Tsukamoto et al., the clock provides unique values to the access controller, which in turn supplies data to the storage device).

Regarding claim 85, Boutaud et al. as modified by Tsukamoto et al. teaches wherein the preprogrammed bit altering scheme is based upon at least one of a serial number or a random number (see fig. 2, ref. num 27 of Tsukamoto et al., the clock is random).

Claims 76-80 and 87-90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (U.S. Patent No. 5,177,786) in view of Tsukamoto et al. (U.S. Patent No. 5,796,828).

Regarding claim 76, Kang teaches an apparatus for storing and retrieving digital video data, comprising:

- An interface couple to a system bus and configured to receive from the system bus a plurality of data bits arranged in a data bit pattern (fig. 3, ref. num 1); and
- A plurality of multiplexers (fig. 3, ref. num 100), each configured to receive each of the plurality of data bits in the data bit pattern and to select a unique one of the data bits according to a preprogrammed bit scrambling scheme (col. 5, lines 10-17), the output of each of the plurality of multiplexers being combined to form an scrambled data bit pattern (col. 5, lines 18-21).

Kang does not teach a storage device coupled to the interface and configured to store the scrambled data bit pattern.

Tsukamoto et al. teaches a storage device coupled to the interface and configured to store the scrambled data bit pattern (fig. 2, ref. num 23A, 24, and 40).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine a storage device for storing the scrambled bit pattern, as taught by Tsukamoto et al., with the apparatus of Kang. It would have been obvious for such modifications because in a DVR application, data bits are required to be stored for later retrieval and viewing. Storing the bits in a scrambled form prevents anyone from illegally viewing the program.

Regarding claims 77 and 78, Kang as modified by Tsukamoto et al. teaches wherein the plurality of multiplexers are implemented in at least one of a hardware device, discrete logic device, or a software device (see fig. 3, ref. num 100 of Kang), wherein the hardware device is at least one of a field-programmable gate array, or an ASIC (the examiner takes official notice that the hardware device is a FPGA or an ASIC because the hardware device could be swapped for another FPGA or ASIC if security were to be compromised.).

Regarding claim 79, Kang as modified by Tsukamoto et al. teaches wherein the preprogrammed bit scrambling scheme is based upon at least one of a serial number or a random number (see fig. 3, ref. num 12 of Kang).

Regarding claim 80, Kang as modified by Tsukamoto et al. teaches wherein the plurality of multiplexers are each further configured to receive, from the storage device, each of the plurality of data bits in the scrambled data bit pattern and to select a unique one of the data bits according to the preprogrammed bit scrambling scheme, the output of each of the plurality of multiplexers being combined to restore the data bit pattern (see fig. 4, ref. num 100 and col. 5, line 59 through col. 6, line 35 of Kang).

Regarding claim 87, Kang teaches a method for storing and retrieving digital video data within a storage device, comprising:

- Receiving data bits across a bus, the data bits forming a bit pattern (fig. 1, ref. num 1);
- Inputting into at least one multiplexer, each of the data bits forming the bit pattern (fig. 3, ref. num 100 and col. 5, lines 10-12);
- Scrambling the bit pattern to form a scrambled bit pattern by selecting a unique one of the data bits in each of the at least one multiplexer based upon a preprogrammed data scrambling scheme to form the scrambled bit pattern (col. 5, lines 13-21);
- Restoring the scrambled bit pattern to the bit pattern by inputting into the at least one multiplexer, each of the data bits of the scrambled bit pattern, and selecting a unique one of the data bits of the scrambled bit pattern based upon the preprogrammed data scrambling scheme (fig. 4, ref. num 100 and col. 5, line 59 through col. 6, line 35); and
- Outputting the restored data bits (fig. 4, ref. num 6).

Kang does not teach storing the scrambled bit pattern.

Tsukamoto et al. teaches storing the scrambled bit pattern (fig. 2, ref. num 23A, 24, and 40).

Regarding claim 88, Kang as modified by Tsukamoto et al. teaches wherein the scrambling and the restoring are preformed by one of a discrete logic device, a software device, a FPGA, or an ASIC (see fig. 3, ref. num 100 of Kang).

Regarding claim 89, Kang as modified by Tsukamoto et al. teaches wherein the scrambling and the restoring are unique to the hardware platform (see fig. 2, ref. num 27 of Tsukamoto et al., the clock provides unique values to the access controller, which in turn supplies data to the storage device).

Regarding claim 90, Kang as modified by Tsukamoto et al. teaches wherein the preprogrammed data scrambling scheme is based upon at least one of a serial number or a random number generator (see fig. 3, ref. num 12 of Kang).

Claims 75, 81, 86, and 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang (USPN '786) in view of Tsukamoto et al. (USPN '828), and further in view of Boutaud et al. (USPN '927).

Claims 75, 81, 86, and 91 add a second set of multiplexers for the purpose of either taking the scrambled data bits and further altering them, or taking the altered bits and further scrambling them. Therefore, the combination of Kang, Tsukamoto et al., and Boutaud et al. teaches the following claim limitations.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine further altering/scrambling of previously scrambled/altered data. It would have been obvious for such modifications because a second round of protection further protects the data. Merely altering the bits may not be enough to deter a usurper from gaining improper access to the set-top box.

Regarding claim 75, Kang as modified by Tsukamoto et al./Boutaud et al. teaches further comprising a second plurality of multiplexers, each configured to receive each of the data bits in the altered data bit pattern and to select a unique one of the data bits in the altered data bit pattern according to a preprogrammed bit scrambling scheme to output an altered and scrambled bit pattern (see col. 5, lines 10-17 of Kang), and wherein the storage device is configured to store the altered and scrambled bit pattern (see fig. 2, ref. num 23A, 24, and 40 of Tsukamoto et al.).

Regarding claim 81, Kang as modified by Tsukamoto et al./Boutaud et al. teaches further comprising a second plurality of multiplexers, each configured to receive each of the data bits in the scrambled data bit pattern and its inverse, and configured to output one of the associated one of the plurality of data bits or its inverse according to a preprogrammed bit altering scheme (see fig. 10D, ref. num 4380 and 4390 of Boutaud et la.), and wherein the storage device is configured to store the scrambled and altered bit pattern (see fig. 2, ref. num 23A, 24, and 40 of Tsukamoto et al.).

Regarding claim 86, Kang as modified by Tsukamoto et al./Boutaud et al. teaches further comprising:

- Scrambling the altered data bits prior to storing to form an altered and scrambled bit pattern by inputting into at least one second multiplexer each of the data bits forming the altered bit pattern and selecting a unique one of the altered data bits according to a preprogrammed bit scrambling scheme to form an altered and scrambled bit pattern (see col. 5, lines 10-17 of Kang);
- Storing the altered and scrambled bit pattern (see fig. 2, ref. num 23A, 24, and 40 of Tsukamoto et al.); and
- Restoring the altered and scrambled bit pattern to the altered bit pattern by inputting into the at least one second multiplexer each of the altered and scrambled data bits and selecting a unique one of the altered and scrambled data bits according to the preprogrammed bit scrambling scheme to for the altered/scrambled bit pattern (see fig. 2, ref. num 25 of Tsukamoto et al., the reverse process if performed).

Regarding claim 91, Kang as modified by Tsukamoto et al./Boutaud et al. teaches further comprising:

- Altering the scrambled data bits prior to storing to form a scrambled and altered bit pattern by inputting each of the data bits of the scrambled bit pattern and its inverse into an associated one of at least one second multiplexer and selecting one of the data bits or its inverse based upon a preprogrammed data altering

scheme to form a scrambled and altered data pattern (see fig. 10D, ref. num 4380 and 4390 of Boutaud et al.);

- Storing the scrambled and altered bit pattern (see fig. 2, ref. num 23A, 24, and 40 of Tsukamoto et al.); and
- Restoring the scrambled and altered bit pattern to the scrambled bit pattern by inputting into the at least one second multiplexer an associated one of the data bits of the altered and scrambled data pattern and its inverse, and selecting data bits of the altered and scrambled data pattern or its inverse according to the preprogrammed bit altering scheme to form the scrambled bit pattern (see fig. 2, ref. num 25 of Tsukamoto et al., the reverse process is performed).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon S. Hoffman whose telephone number is 571-272-3863. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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